(12) UK Patent Application (19) GB (11) 2 307 616 (13) A

(43) Date of A Publication 28.05.1997

(21) Application No 9624471.0

(22) Date of Filing 25.11.1996

(30) Priority Data
(31) 9543583 (32) 24.11.1995 (33) KR

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(51) INT CL^6
H04N 11/04

(52) UK CL (Edition O)
H4F FD1B9 FD1D1 FD12X FD3P FD3R FD3T FD30K FD79 FRW

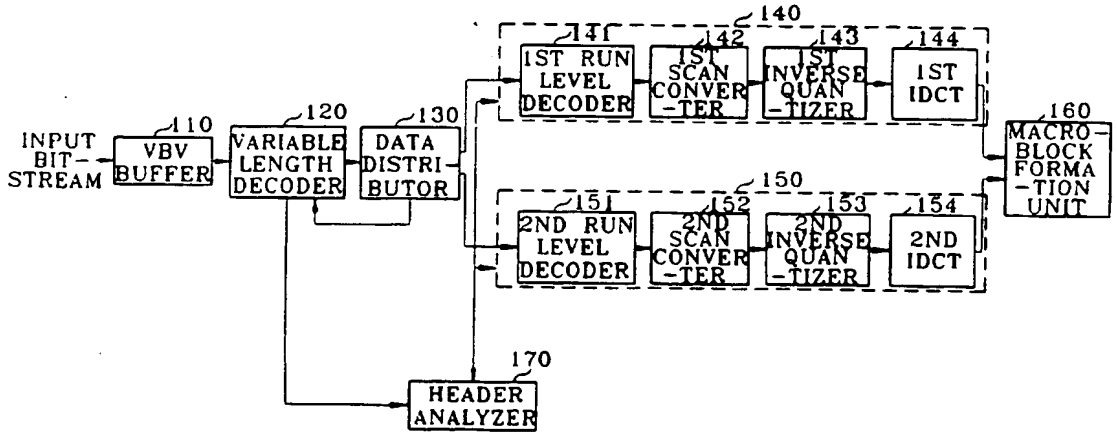
(56) Documents Cited
GB 2240231 A WO 95/32578 A2

(58) Field of Search
UK CL (Edition O) H4F FRC FRD FRG FRM FRP FRR FRT FRW FRX
INT CL^6 H04N 7/00 7/24 7/26 7/32 7/34 7/36 7/46 7/48 7/50 11/00 11/02 11/04
Online:WPI

(54) Apparatus for decoding MPEG video bitstream

(57) An apparatus for decoding a video bitstream according to the MPEG standard restores variable length decoded data at a processing speed required in a high-speed system. The decoding apparatus includes a variable length decoder 120 outputting header data and symbols, a data distributor 130 alternately outputting the symbols in units of a block via two output terminals, first and second restorers 140, 150 individually connected to the two output terminals of the data distributor 130 for restoring the input symbols in response to an encoding indication signal for indicating whether each block is encoded, a header analyser 170 for receiving the header data from the variable length decoder 120 and outputting the encoding indication signal, and a macroblock formation unit 160 for reconstructing blocks of the data restored by the first and second restorers 140, 150 into a macroblock.

FIG. 1



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIG. 1

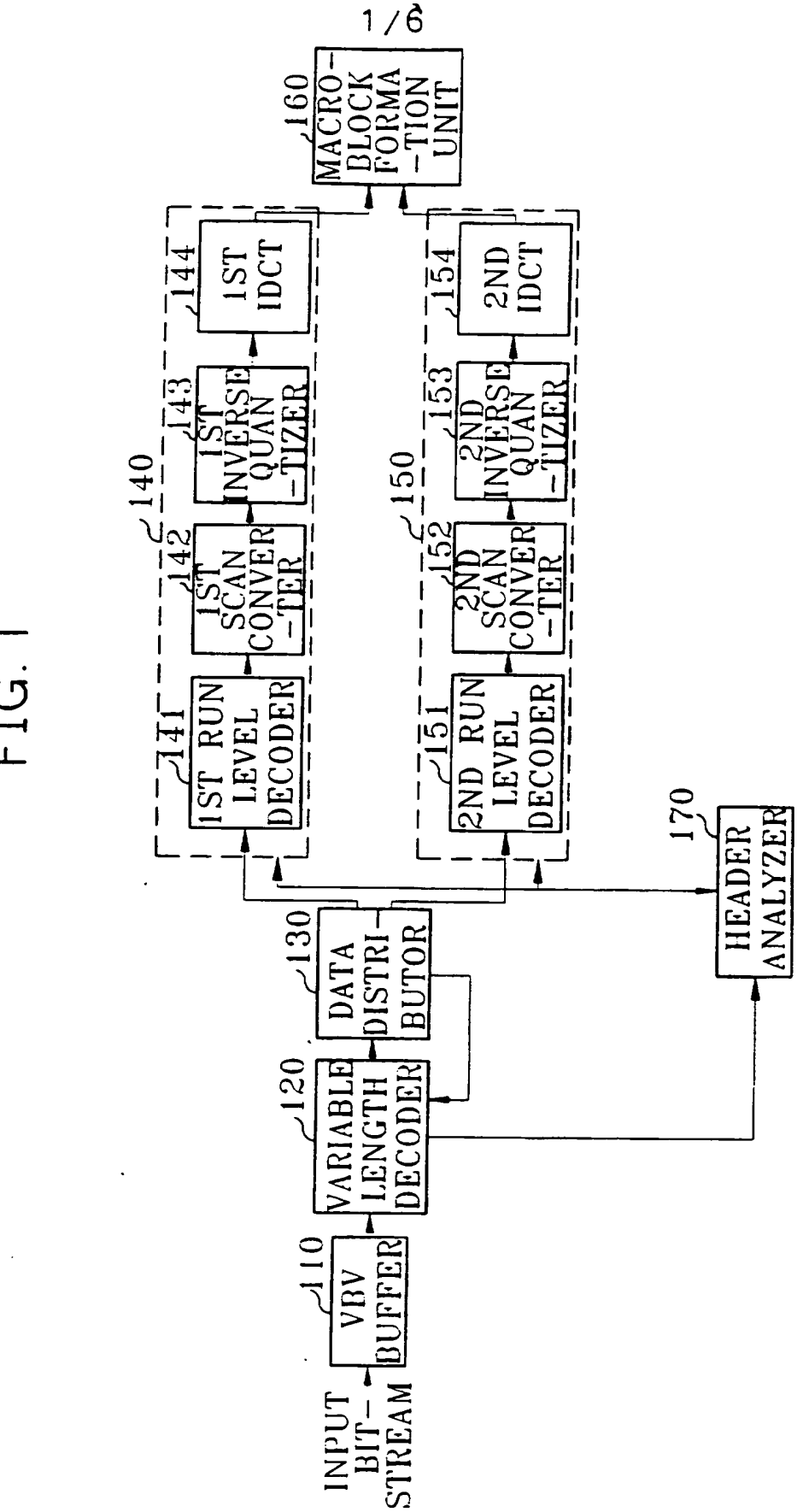

INPUT BIT-STREAM
110 VBV BUFFER
120 VARIABLE LENGTH DECODER
130 DATA DISTRI-BUTOR
140
141 1ST RUN LEVEL DECODER
142 1ST SCAN CONVER-TER
143 1ST INVERSE QUAN-TIZER
144 1ST IDCT
150
151 2ND RUN LEVEL DECODER
152 2ND SCAN CONVER-TER
153 2ND INVERSE QUAN-TIZER
154 2ND IDCT
160 MACRO-BLOCK FORMA-TION UNIT
170 HEADER ANALYZER

FIG. 2

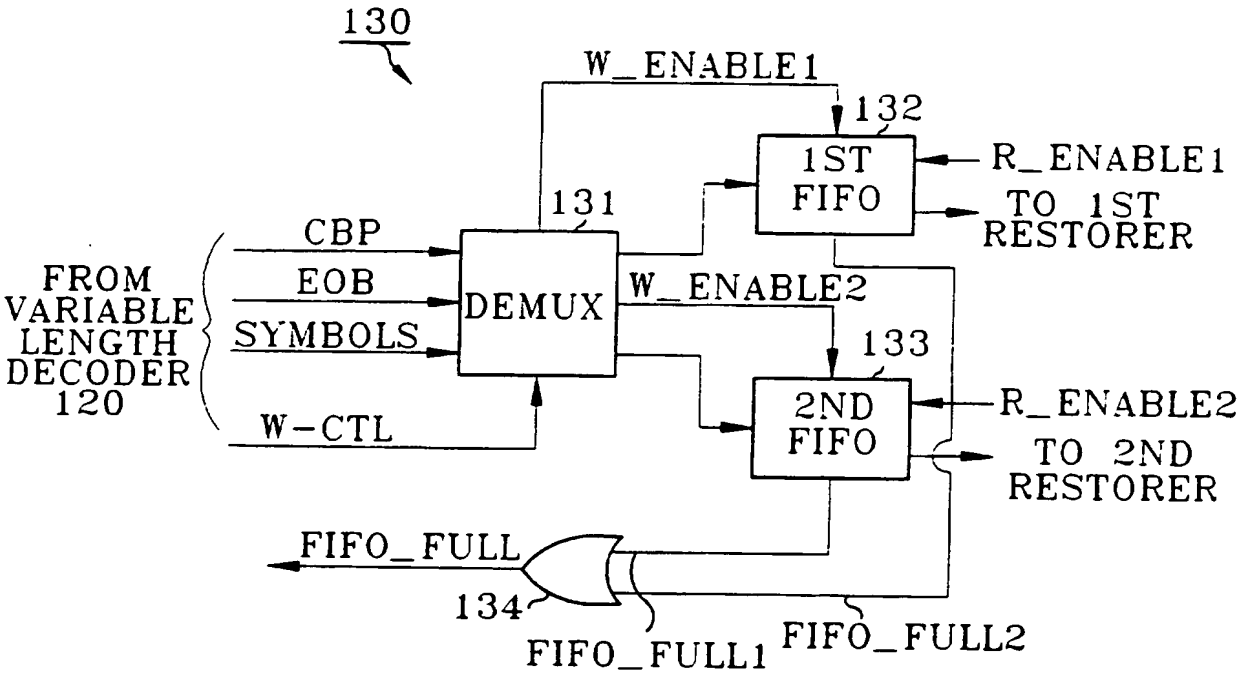


FIG. 3

Y1	Y3	Cu
Y2	Y4	Cv

FIG. 4

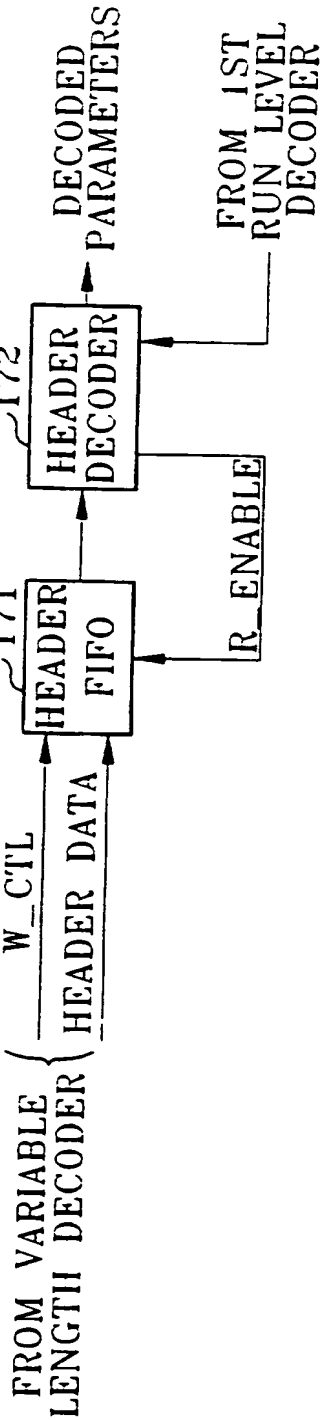

170
DECODED PARAMETERS
FROM 1ST RUN LEVEL DECODER
172
HEADER DECODER
171
HEADER FIFO
R_ENABLE
W_CTL
HEADER DATA
FROM VARIABLE LENGTH DECODER

FIG. 5

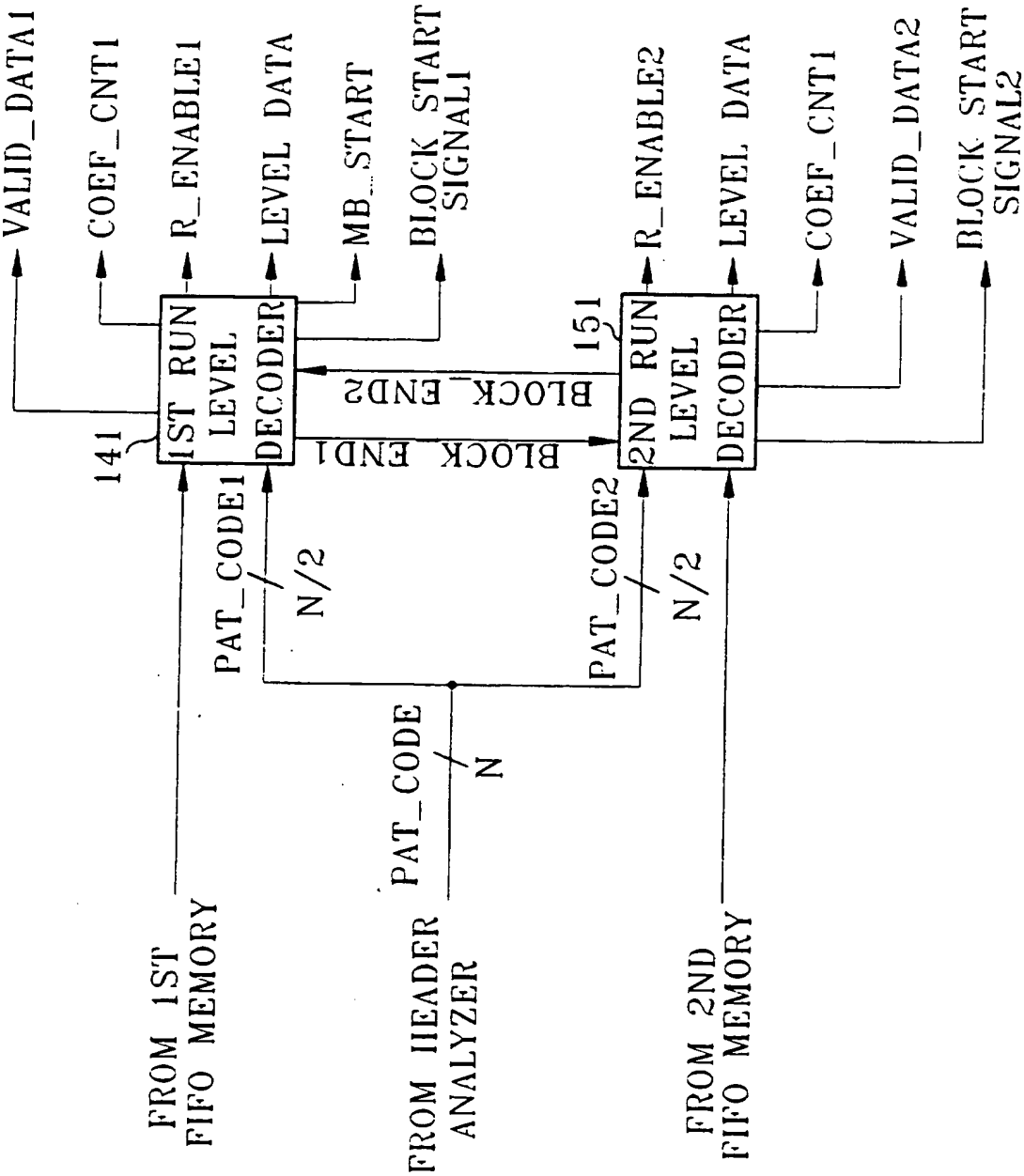

VALID_DATA1
COEF_CNT1
R_ENABLE1
LEVEL DATA
MB_START
BLOCK START SIGNAL1
141
1ST RUN LEVEL DECODER
BLOCK_END2
BLOCK_END1
151
2ND RUN LEVEL DECODER
R_ENABLE2
LEVEL DATA
COEF_CNT1
VALID_DATA2
BLOCK START SIGNAL2
PAT_CODE1
N/2
PAT_CODE2
N/2
PAT_CODE
N
FROM 1ST FIFO MEMORY
FROM HEADER ANALYZER
FROM 2ND FIFO MEMORY

FIG. 6

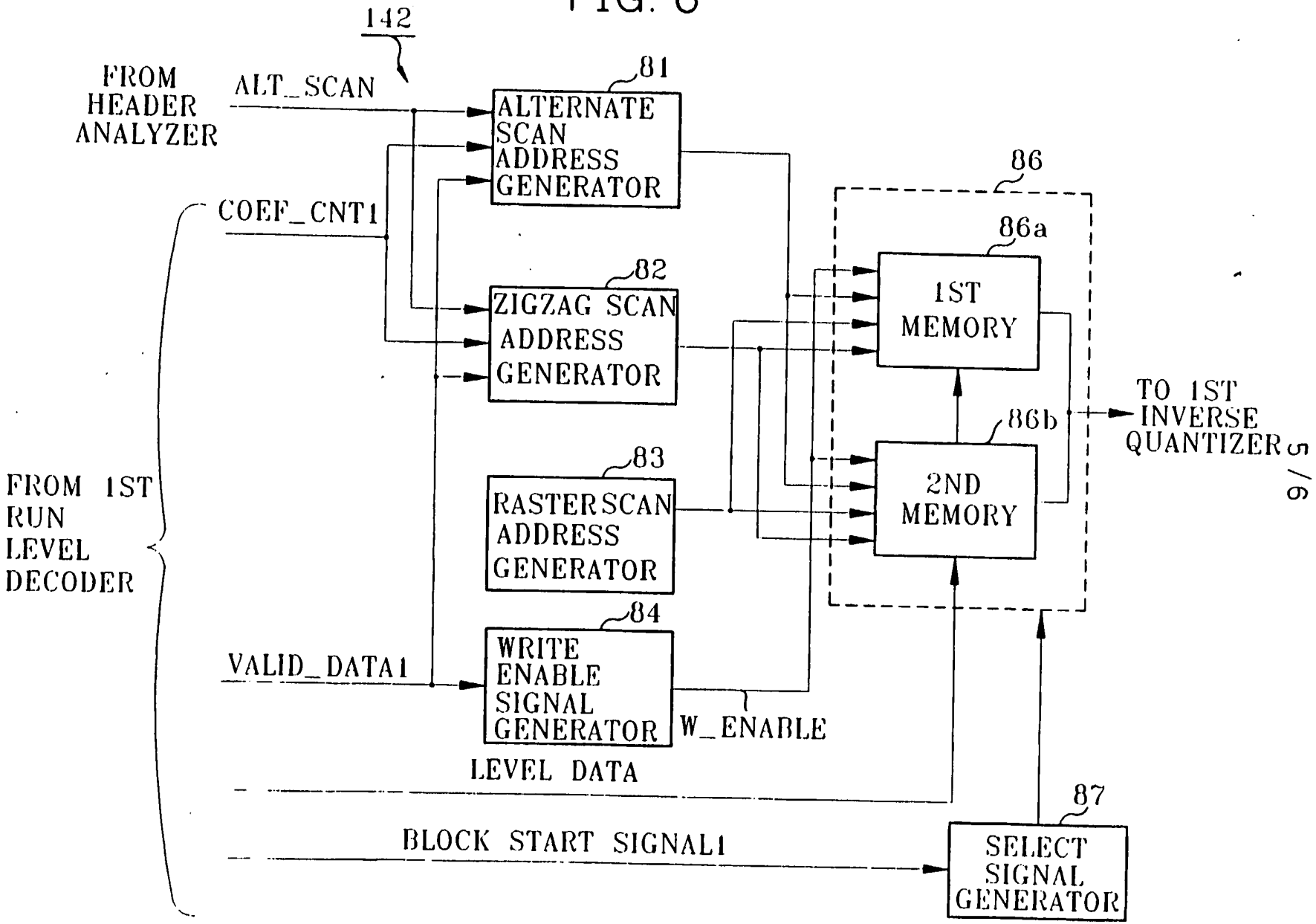
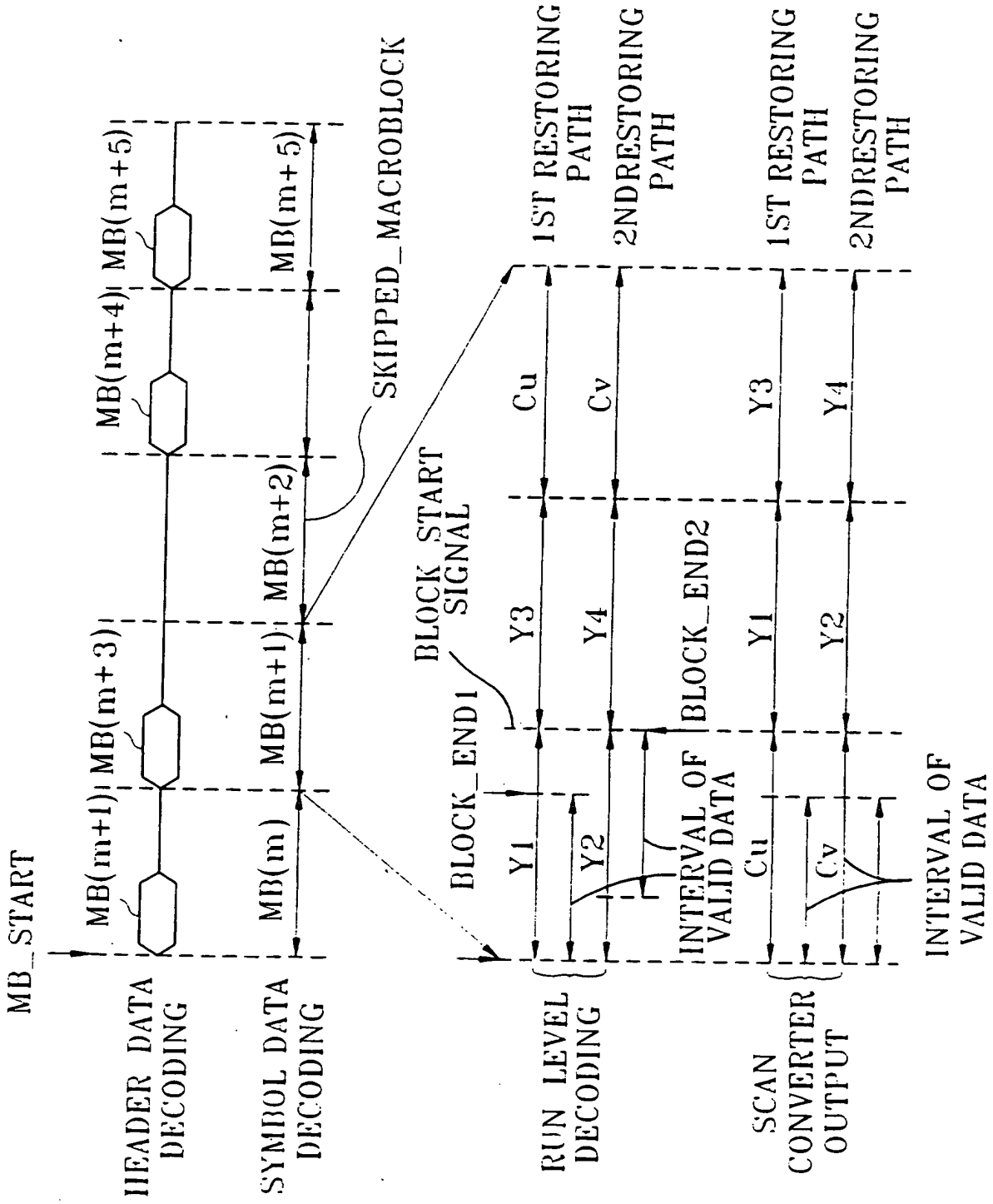

142
FROM HEADER ANALYZER
ALT_SCAN
81
ALTERNATE SCAN ADDRESS GENERATOR
COEF_CNT1
82
ZIGZAG SCAN ADDRESS GENERATOR
83
RASTER SCAN ADDRESS GENERATOR
84
WRITE ENABLE SIGNAL GENERATOR
VALID_DATA1
W_ENABLE
86
86a
1ST MEMORY
86b
2ND MEMORY
TO 1ST INVERSE QUANTIZER
FROM 1ST RUN LEVEL DECODER
LEVEL DATA
BLOCK START SIGNAL1
87
SELECT SIGNAL GENERATOR

FIG. 7


MB_START
HEADER DATA DECODING
SYMBOL DATA DECODING
RUN LEVEL DECODING
SCAN CONVERTER OUTPUT
MB(m+1)
MB(m+3)
MB(m)
MB(m+1)
MB(m+2)
MB(m+4)
MB(m+5)
MB(m+5)
SKIPPED_MACROBLOCK
BLOCK_START SIGNAL
BLOCK_END1
BLOCK_END2
Y1
Y2
Y3
Y4
Cu
Cv
INTERVAL OF VALID DATA
1ST RESTORING PATH
2NDRESTORING PATH

APPARATUS FOR DECODING MPEG VIDEO BITSTREAM

The present invention relates to an apparatus for decoding a video bitstream, and more particularly, to an apparatus for decoding an MPEG (moving pictures experts group) video bitstream which can perform a decoding operation for a video bitstream on a real-time basis in a system such as a high-definition TV (HDTV) requiring a high-speed processing.

A system such as a HDTV requiring a high-speed processing operation, requires a system clock of at least 100MHz in order to decode an input bitstream when considering picture size and header information. Also, a system clock of 110-120 MHz is required considering an interface between the whole components in a decoder.

However, when a decoder is implemented by using conventional components, it is difficult to expect a stable decoding as well as to perform a decoding operation at desired speed.

With a view to solving or reducing the above problem, it is an aim of embodiments of the present invention to provide an apparatus for decoding an MPEG video bitstream via a plurality of paths which can process a video bitstream according to the MPEG standard on a real-time basis and reduce a burden of a system clock according to real-time processing by decoding blocks constituting each macroblock via different decoding paths.

According to a first aspect of the present invention, there is provided an apparatus for decoding a video bitstream according to the MPEG standard, the decoding apparatus comprising: variable length decoding means for

variable length decoding the video bitstream and outputting header data and symbols obtained by the variable length decoding; a data distributor for receiving the output of said variable length decoding means and alternately outputting the symbols in units of a block via two output terminals; first and second restoring means individually connected to said two output terminals of said data distributor for restoring the input symbols in response to an encoding indication signal for indicating whether each block is encoded; a header analyzer for receiving the header data from said variable length decoding means and analyzing the received header data and outputting said encoding indication signal; and macroblock formation means for reconstructing blocks of the data restored by said first and second restoring means into a macroblock.

Preferably, said variable length decoding means outputs a block end signal together with the symbols, and said data distributor comprises a demultiplexer for alternately supplying the input symbols to said first and second restoring means in units of a block based on said block end signal.

Preferably, said data distributor comprises: a first FIFO memory interposed between the output of said demultiplexer and the input of said first restoring means, for storing the symbols supplied from said variable length decoding means and generating a first data fullness signal; a second FIFO memory interposed between the output of said demultiplexer and the input of said second restoring means, for storing the symbols supplied from said variable length decoding means and generating a second data fullness signal; and an OR gate for logically combining said first and second data fullness signals, and

wherein said variable length decoding means temporarily interrupts data supply to said data distributor if the output of said OR gate indicates that one of said first and second FIFO memories is full.

Preferably, said first restoring means decodes the symbols stored in said first FIFO memory based on an encoding indication signal and said second restoring means decodes the symbols stored in said second FIFO memory based on the encoding indication signal, and one of said first and second restoring means generates a macroblock decoding start signal for the next macroblock based on a point in time of completion of the run level decoding with respect to the final block in each macroblock.

Preferably, said each restoring means comprises: a run level decoder for down-counting run data constituting the symbol, outputting corresponding level data whenever the down-count is completed, reading the next symbol from said corresponding FIFO memory, and generating a block start signal indicating decoding start with respect to each block; a write address generator for generating a write address in response to the down-count result of said run level decoding means; a read address generator for generating a read address in response to the block start signal of said run level decoding means; and a memory for recording the level data output from said run level decoding means according to the write address of said write address generator and outputting the recorded level data according to the read address of said read address generator.

Preferably, said read address generator generates read addresses for reading the data stored in said memory by one block size in response to the block start signal,

and said memory stores the data value of "0" if the down-count result indicates that the down-count is proceeding, while said memory stores the level data supplied from said run level decoding means if the down-count result indicates that the down-count has been completed.

Preferably, said header analyzer comprises: a FIFO memory for storing the header data output from said variable length decoding means; and means for reading the header data of the corresponding macroblock from said FIFO memory and outputting the read header data.

According to a second aspect of the invention, there is provided an apparatus for decoding a video bitstream according to the MPEG standard, the decoding apparatus comprising: variable length decoding means for receiving the bitstream and outputting variable length decoded data; a data distributor for receiving the output of said variable length decoding means and outputting symbols in units of a block via a plurality of output terminals; plural restoring means connected to the plurality of outputs of said data distributor for restoring input symbols in response to an encoding indication signal; a header analyzer, connected to the variable length decoding means and adapted to receive header data therefrom, for analyzing the received header data and outputting the encoding indication signal; and macroblock formation means for reconstructing blocks of data restored by the restoring means into a macroblock.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a decoding apparatus according to a preferred embodiment of the present invention;

Figure 2 is a detailed block diagram of a data distributor of the Figure 1 embodiment;

Figure 3 is a view for explaining a macroblock;

Figure 4 is a detailed block diagram of a header analyzer of the embodiment of Figure 1;

Figure 5 is a detailed block diagram of run level decoders of the embodiment of Figure 1;

Figure 6 is a detailed block diagram of a scan converter of the embodiment of Figure 1; and

Figure 7 is a timing diagram for explaining the operation of the Figure 1 apparatus.

A preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings.

Referring to Figure 1 illustrating an embodiment of the presen invention, a video buffering verifier (VBV) buffer 110 receives a video bitstream according to the MPEG-2 standard. Since the VBV buffer 110 is well known to a person skilled in the art as it follows the MPEG-2 standard, a detailed description thereof will be omitted. A variable length decoder 120 performs a variable length decoding operation with respect to the video bitstream output from the VBV buffer 110. The variable length decoder 120 supplies symbols obtained by the variable

length decoding to a data distributor 130. The variable length decoder 120 supplies header data obtained from the input video bitstream to a header analyzer 170. The variable length decoder 120 also supplies part of the header data obtained from the video bitstream to the data distributor 130. The data distributor 130 distributes the symbols supplied from the variable length decoder 120 in units of a block to a first restorer 140 and a second restorer 150 constituting a first restoring path and a second restoring path, respectively, on the basis of the applied header data. The header analyzer 170 analyzes the header data supplied from the variable length decoder 120 and outputs various parameters necessary for data restoration of the Figure 1 apparatus. Both the first and second restorers 140 and 150 restore the symbols supplied from the data distributor 130 according to the parameters output from the header analyzer 170, and output the restored data to a macroblock formation unit 160. The macroblock formation unit 160 reconstructs the blocks of the received data into a macroblock.

The detailed structure and operation of the Figure 1 apparatus in connection with signal lines and components which are shown in Figure 1 will be described in more detail with reference to Figures 2 through 7.

Figure 2 is a detailed block diagram of the data distributor 130 of Figure 1. The data distributor 130 includes a demultiplexer 131 which receives the symbols and header data supplied from the variable length decoder 120. The demultiplexer 131 receives a coded block pattern (CBP) signal, an end of block (EOB) signal, the symbols and a write control (W_CTI), which are output from the variable length decoder 120. The CBP and the EOB follows the MPEG standard, which is header data contained in the

video bitstream received in the Figure 1 apparatus. The CBP signal is header data which is transmitted only in the encoded inter-macroblock, and indicates which block is encoded among the respective inter-macroblocks. The write control signal W_CTL is generated in the variable length decoder 120, and is a signal indicating a write point in time with respect to the output data. The demultiplexer 131 uses the CBP signal, the EOB signal and the write control signal in order to separate blocks composed of the input symbols. In more detail, the demultiplexer 131 identifies blocks of the encoded symbols according to the CBP signal and the EOB signal. In particular, the demultiplexer 131 distributes the identified blocks to first and second first-in-first-out (FIFO) memories 132 and 133, based on the structure of the macroblock shown in Figure 3. Figure 3 is a view for explaining a macroblock which is involved with a 4:2:0 format of a picture. The macroblock is composed of six blocks, in which one macroblock is encoded in sequence with Y1, Y2, Y3, Y4, Cu and Cv. Here, Y1-Y4 represent luminance blocks and Cu and Cv represent chrominance blocks. Therefore, the demultiplexer 131 supplies the blocks Y1, Y3 and Cu of Figure 3 to the first FIFO memory 132, and supplies the blocks Y2, Y4 and Cv to the second FIFO memory 133. The demultiplexer 131 generates a first write enable signal W_ENABLE1 according to the write control signal when data is supplied to the first FIFO memory 132, and generates a second write enable signal W_ENABLE2 according to the write control signal when data is supplied to the second FIFO memory 133. The demultiplexer 131 also uses the above-described encoded block pattern (CBP) in order to prevent the symbols from being wrongly distributed by the block which is not encoded in the inter-macroblock.

The first FIFO memory 132 stores the symbols applied together with the first write enable signal W_ENABLE1 from the demultiplexer 131, and the second FIFO memory 133 stores the symbols applied together with the second write enable signal W_ENABLE2 from the demultiplexer 131. The first and second FIFO memories 132 and 133 output fullness signals FIFO_FULL1 and FIFO_FULL2 indicating data fullness to an OR gate 134, if the individually stored data exceeds a predetermined amount of the data. The OR gate 134 logically sums the first and second fullness signals FIFO _FULL1 and FIFO_FULL2, and outputs the resultant fullness signal FIFO_FULL to the variable length decoder 120. The variable decoder 120 judges data fullness of the first and second FIFO memories 132 and 133, based on the fullness signal FIFO_FULL, and accordingly controls the amount of the data to be supplied to the demultiplexer 120. That is, if the fullness signal FIFO_FULL indicates that the first or second FIFO memory 132 or 133 is full of a predetermined amount of data or more, the variable length decoder 120 interrupts the data output to the data distributor 130. Meanwhile, if the fullness signal FIFO FULL indicates that the first or second FIFO memory 132 or 133 is not full of a predetermined amount of data or more, the variable length decoder 120 performs the data supply to the data distributor 130.

Also, the first FIFO memory 132 outputs the stored data to the first restorer 140 if a first read enable signal R_ENABLE1 is applied from a first run level decoder 141. The second FIFO memory 133 outputs the stored data to the second restorer 150 if a second read enable signal R_ENABLE2 is applied from a second run level decoder 142.

The header analyzer 170 shown in Figure 4 includes a header FIFO memory 171 and a header decoder 172. The

header FIFO memory 171 stores the header data transmitted from the variable length decoder 120 together with the write control signal W_CTL, and outputs the stored data according to the read enable signal R_ENABLE. The header decoder 172 decodes the data output from the header FIFO memory 171 and generates a plurality of parameters including an encoding indication signal and a scan type select signal ALT_SCAN. Here, the encoding indication signal PAT_CODE is needed for decoding the symbols in units of a block, and indicates whether each block within each macroblock has been encoded. The scan type select signal ALT_SCAN is a signal for designating a zigzag scan or an alternate scan with respect to each block.

The header decoder 172 generates a read enable signal R_ENABLE at the time when a macroblock decoding start signal MB_START shown in Figure 7 is generated, starts reading of the header data of a corresponding macroblock MB(M+1), and interrupts generation of the read enable signal R_ENABLE if the header data has been completely read. The header decoder 172 generates again a read enable signal R_ENABLE at the time when a next macroblock decoding start signal MB_START is generated, and reads the header data of the corresponding macroblock ME(m+2). The header decoder 172 decodes the header data read from the header FIFO memory 171. Particularly, the header decoder 172 decodes the header data of the macroblock which goes at least earlier than the data of the macroblock which is restored by the first and second restorers 140 and 150. The header decoder 172 supplies the encoding indication signal PAT_CODE obtained by the decoding to the first and second restorers 140 and 150 whenever the macroblock decoding start signal MB_START is applied from the first run level decoder 141 to be described later. Therefore, the macroblock to be restored by the first and second

restorers 140 and 150 becomes a macroblock which goes just previously in advance of the macroblock corresponding to the macroblock decoding start signal MB_START.

Figure 5 is a detailed block diagram of first and second run level decoders 141 and 151 of Figure 1. If the encoding indication signal PAT_CODE output from the header analyzer 172 indicates that a block is an encoded block, the first and second run level decoders 141 and 151 perform run level decoding with respect to the block. The encoding indication signal PAT_CODE indicates which one of an intra-macroblock, an inter-macroblock, a skipped macroblock and a non-coded macroblock is a macroblock to which blocks belong, and whether the blocks belonging to each macroblock have been encoded. The encoding indication signal PAT_CODE has a bit value of "1" for an encoded block and a bit value of "0" for the non-encoded block. Such an encoding indication signal PAT_CODE is received via N bus lines from the header decoder 172, and a bus width is varied according to a data format of the macroblock. For example, the bus width becomes 6 bits in case of a 4:2:0 format, 8 bits in case of a 4:2:2 format, and 12 bits in case of a 4:4:4 format. Therefore, the first and second run level decoders 141 and 151 receive the encoding indication signals PAT_CODE1 and PAT_CODE2 via three bus lines, respectively.

The first and second run level decoders 141 and 151 generate a block start signal, based on the data received from the first and second FIFO memories 132 and 133, respectively, and start run level decoding with respect to each block based on the block start signal. The first and second run level decoders 141 and 151 start run level decoding of the symbols of each block from the point in time of generation of the block start signal shown in

Figure 7. However, the point in time of decoding with respect to each block is varied according to a degree of the data storage in the first and second FIFO memories 132 and 133. As an example, when the second FIFO memory 133 is empty, the second run level decoder 151 does not start run level decoding in response to the block start signal and awaits until the second FIFO memory 133 is filled with the symbols of one block, to then start run level decoding. Thus, the first and second run level decoders 141 and 151 complete the run level decoding at different points in time. Accordingly, the first and second run level decoders 141 and 151 generate block encoding end signals BLOCK_END1 and BLOCK_END2 indicating that run level decoding is completed with respect to the block of the input symbols, and give and take the generated block decoding end signals to and from each other, respectively. As can be seen from Figure 7, the first and second run level decoders 141 and 151 make the points in time of generation of the block start signals coincident with each other. As a result, a valid data intervals with respect to the output of the scan converter become coincident with each other. As an example of the different run level decoding end points in time, Figure 7 shows the different points in time of generation of the block decoding end signals BLOCK_END1 and BLOCK_END2 in connection with the run level decoding. The first and second run level decoders 141 and 151 compare the generated block decoding end signal with the received block decoding end signal, and generates a block start signal for the next block based on the block decoding end signal at the point in time which is relatively later. The first run level decoder 141 generates a macroblock decoding start signal MB_START to be supplied to the header analyzer 170, based on the point in time of generation of the final block start signal with respect to each macroblock.

Meanwhile, the operation of the first run level decoder 141 will be described with respect to the run level decoding. The first run level decoder 141 generates a first data valid signal VALID_DATA1 of a high-level state during the time when the run level decoded data is output, and down-counts the run data of each symbol. The first run level decoder 141 outputs the count value COEF_CNT1 during the time when down-counting is performed, and outputs level data corresponding to the run data of which the down-count is completed, to the first scan converter 142. The first run level decoder 141 also generates a first read enable signal R_ENABLE1 whenever down-count with respect to each run data is completed, and the first FIFO memory 132 responding to the generated first read enable signal R_ENABLE1 supplies the next symbol data to the first run level decoder 141. Such an operation in connection with the run level decoding is performed in the same manner even in the second run level decoder 151. The resultant second data valid signal VALID_DATA2, count value COEF_CNT1 and level data are output to the second scan converter 152. The second read enable signal R_ENABLE2 is transmitted to the second FIFO memory 133.

Figure 6 is a detailed block diagram of a first scan converter 142 which receives the outputs of the first run level decoder 141. Since the first and second scan converters 142 and 152 have the same constitution as that of Figure 6, respectively, the detailed description of only the first scan converter 142 will follow.

In Figure 6, an alternate scan address generator 81 and a zigzag scan address generator 82 receive the scan type select signal ALT_SCAN of the header decoder 172 of Figure 4, and are active according to the value of the scan type select signal ALT_SCAN. If the first data valid

signal VALID__DATA1 is applied to the alternate scan address generator 81, the zigzag scan address generator 82 and an enable signal generator 84, the alternate scan address generator 81 or the zigzag scan address generator 82 generate scan addresses during the time when the first data valid signal VALID_DATA1 is applied. As an example, if the value of the scan type select signal ALT_SCAN is "1", the zigzag scan address generator 82 generates san addresses, and if the value thereof is "0", the alternate scan address generator 81 generates scan addresses. The enable signal generator 84 generates a write enable signal W_ENABLE and supplies the same to a memory bank 86. The block start signal is applied to a raster scan address generator 83 and a select signal generator 87. The select signal generator 87 generates a memory change signal CHANGE based on the received block start signal. A first memory 86a or a second memory 86b in the memory bank 86 stores the data or outputs the stored data according to the value of the memory change signal CHANGE, in which when the first memory 86a stores the input data, the second memory 86b outputs the stored data. Also, if the value of the memory change signal CHANGE is changed, the operation is reversed. The first and second memories 86a and 86b are designed to have capacities of storing one block of the run level decoded data.

The alternate scan address generator 81 or the zigzag scan address generator 82 generates a memory write address for one block size, that is, the size of 8x8 pixels according to the scan type select signal ALT_SCAN and the count value COEF_CNT1. The first or second memory 86a or 86b is selected to perform a write operation according to the memory change signal of the select signal generator 87, and stores the level data supplied from the first run level decoder 141 according to he memory write address

applied from the address generator 81 or 82. Finally, the first or second memory 86a or 86b stores "0" at the storage location corresponding to the count value COEF_CNT1, and stores the level data at the next storage location.

The raster scan address generator 83 increases an internal counter from 0 to 63 in response to the block start signal, to generate a read address, and repeat an up-counting operation and a read address generation operation starting from 0 if the count value reaches 63. The first or second memory 86a or 86b which receives the read address outputs the stored data to a first inverse quantizer 143.

The first inverse quantizer 143 and a first inverse discrete cosine transformer (IDCT) 144 perform inverse quantization and inverse discrete cosine transformation in turn with respect to the output of the first scan converter 142, and output the resultant data to the macroblock formation unit 160. A second inverse quantizer 153 and a second inverse discrete cosine transformer (IDCT) 154 perform inverse quantization and inverse discrete cosine transformation in turn with respect to the output of the second scan converter 52, and output the resultant data to the macroblock formation unit 160. Since the operations of the inverse quantizers 143 and 153 and the IDCTs 144 and 154 are well known to one having an ordinary skill in the art, the detailed description thereof will be omitted. The macroblock formation unit 160 of Figure 1 reconstructs the data supplied from the first and second IDCT units 144 and 154 into a prior-to-being-encoded video macroblock.

As described above, the apparatus for decoding the MPEG video bitstream via a plurality of paths restores the blocks constituting each macroblock using the header data contained in the video bitstream via a respectively different restoring path, and reconstructs the restored data into a macroblock size. A system such as a HDTV requiring a high-speed processing can process data on a real-time basis, and can synchronize the data which is separated into two paths for data restoration, based on the valid data, to thereby facilitate hardware implementation.

While only certain embodiments of the invention have been specifically described herein, it will be apparent that numerous modifications may be made thereto without departing from the scope of the invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly

stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. An apparatus for decoding a video bitstream according to the MPEG standard, the decoding apparatus comprising:

variable length decoding means for variable length decoding the video bitstream and outputting header data and symbols obtained by the variable length decoding;

a data distributor for receiving the output of said variable length decoding means and alternately outputting the symbols in units of a block via two output terminals;

first and second restoring means individually connected to said two output terminals of said data distributor for restoring the input symbols in response to an encoding indication signal for indicating whether each block is encoded;

a header analyzer for receiving the header data from said variable length decoding means and analyzing the received header data and outputting said encoding indication signal; and

macroblock formation means for reconstructing blocks of the data restored by said first and second restoring means into a macroblock.

2. The decoding apparatus according to claim 1, wherein said variable length decoding means outputs a block end signal together with the symbols, and said data distributor comprises a demultiplexer for alternately supplying the input symbols to said first and second restoring means in units of a block based on said block end signal.

3. The decoding apparatus according to claim 1 or 2, wherein said data distributor comprises:

a first FIFO memory interposed between the output of said demultiplexer and the input of said first restoring means, for storing the symbols supplied from said variable length decoding means and generating a first data fullness signal;

a second FIFO memory interposed between the output of said demultiplexer and the input of said second restoring means, for storing the symbols supplied from said variable length decoding means and generating a second data fullness signal; and

an OR gate for logically combining said first and second data fullness signals, and

wherein said variable length decoding means temporarily interrupts data supply to said data distributor if the output of said OR gate indicates that one of said first and second FIFO memories is full.

4. The decoding apparatus according to claim 3, wherein said first restoring means decodes the symbols stored in said first FIFO memory based on an encoding indication signal and said second restoring means decodes the symbols stored in said second FIFO memory based on the encoding indication signal, and one of said first and second restoring means generates a macroblock decoding start signal for the next macroblock based on a point in time of completion of the run level decoding with respect to the final block in each macroblock.

5. The decoding apparatus according to claim 4, wherein said each restoring means comprises:

a run level decoder for down-counting run data constituting the symbol, outputting corresponding level data whenever the down-count is completed, reading the next symbol from said corresponding FIFO memory, and generating a block start signal indicating decoding start with respect to each block;

a write address generator for generating a write address in response to the down-count result of said run level decoding means;

a read address generator for generating a read address in response to the block start signal of said run level decoding means; and

a memory for recording the level data output from said run level decoding means according to the write address of said write address generator and outputting the recorded level data according to the read address of said read address generator.

6. The decoding apparatus according to claim 5, wherein said read address generator generates read addresses for reading the data stored in said memory by one block size in response to the block start signal, and said memory stores the data value of "0" if the down-count result indicates that the down-count is proceeding, while said memory stores the level data supplied from said run level decoding means if the down-count result indicates that the down-count has been completed.

7. The decoding apparatus according to claim 4, 5 or 6 wherein said header analyzer comprises:

a FIFO memory for storing the header data output from said variable length decoding means; and

means for reading the header data of the corresponding macroblock from said FIFO memory and outputting the read header data.

8. Decoding apparatus for decoding a video bitstream according to the MPEG standard, the apparatus being substantially as herein described with reference to the accompanying drawings.

9. An apparatus for decoding a video bitstream according to the MPEG standard, the decoding apparatus comprising:

variable length decoding means for receiving the bitstream and outputting variable length decoded data;

a data distributor for receiving the output of said variable length decoding means and outputting symbols in units of a block via a plurality of output terminals;

plural restoring means connected to the plurality of outputs of said data distributor for restoring input symbols in response to an encoding indication signal;

a header analyzer, connected to the variable length decoding means and adapted to receive header data therefrom, for analyzing the received header data and outputting the encoding indication signal; and

macroblock formation means for reconstructing blocks of data restored by the restoring means into a macroblock.

10. Apparatus according to claim 9, further comprising any one or more features from the accompanying claims, description, abstract or drawings, in any combination.

The Patent Office

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Application No: GB 9624471.0
Claims searched: 1 to 10

Examiner: John Donaldson
Date of search: 13 January 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4F(FRC, FRD, FRG, FRM, FRP, FRR, FRT, FRW, FRX)

Int Cl (Ed.6): H04N 7/00, 7/24, 7/26, 7/32, 7/34, 7/36, 7/46, 7/48, 7/50, 11/00, 11/02, 11/04

Other: Online:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	GB 2240231 A (B B C), see abstract	-
A, P	WO 95/32578 A2 (ZORAN), see abstract	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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